CLAIMS

1. A method for manufacturing an integrated circuit, the method comprising:

(i) forming a first layer comprising a first portion and a second portion, wherein the first portion is to provide a first feature of the integrated circuit, and the second portion physically contacts the first portion at the location of the first feature;

(ii) forming a first mask over the first layer, the first mask overlying the first portion but having an opening over the second portion;

(iii) etching the second portion selectively to the first mask to at least partially remove the second portion;

(iv) forming a second mask over the first layer, the second mask covering the first and second portions; and

(v) etching the first layer selectively to the second mask, wherein the etching of the first layer comprises lateral etching of the first layer.

2. The method of Claim 1 wherein the operation (v) is isotropic etching of the first layer.

3. The method of Claim 1 wherein the etching operation (iii) comprises anisotropic etching of the second portion.

4. The method of Claim 1 further comprising, before forming the first layer, forming at least one first structure projecting upward over a semiconductor substrate in the integrated circuit;

wherein the first and second portions are sidewall spacers formed over a sidewall or sidewalls of the first layer.

5. The method of Claim 1 further comprising, before forming the first layer, forming at least one first structure projecting upward over a semiconductor substrate in the integrated circuit, each first structure comprising a first sidewall and a second sidewall;

wherein the first portion of the first layer overlays the first sidewall of the first structure;

wherein the first layer further comprises a third portion over the second sidewall of the first structure;

wherein the operation (v) removes the third portion.

6. The method of Claim 5 wherein the operation (i) comprises anisotropically etching the first layer to form spacers over the first and second sidewalls of the first structure.

7. The method of Claim 5 wherein the first and second sidewalls are dielectric sidewalls.

8. The method of Claim 1 wherein the integrated circuit comprises an additional feature at least partially patterned by the etching operation (iii).

9. The method of Claim 8 wherein the additional feature is a transistor gate.

10. The method of Claim 1 wherein the operation (iii) removes the second portion only partially.

11. The method of Claim 1 wherein the first portion is conductive.

12. An integrated circuit comprising:

a first feature; and

an extension of the fist feature, the extension being formed from the same material as the first feature, the extension being contiguous with the first feature, the extension having a smaller cross sectional area than the first feature.

13. The integrated circuit of Claim 12 further comprising a semiconductor substrate, and a first structure projecting upward over the semiconductor substrate, the first structure comprising a first sidewall;

wherein the first feature overlays the first sidewall of the first structure.

14. The integrated circuit of Claim 13 wherein the extension of the first feature does not project upward as far as the first feature.

15. The integrated circuit of Claim 12 wherein the first feature and the extension are sidewall spacers on the first sidewall.

16. The integrated circuit of Claim 12 wherein the first feature and the extension are conductive.

17. The integrated circuit of Claim 12 wherein the first structure comprises a conductive line, and the first sidewall is dielectric.

18. The integrated circuit of Claim 17 wherein the conductive line provides control gates to a plurality of memory cells, the first structure also comprises conductive floating gates of the memory cells, and the first feature is a wordline for the memory cells.